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09/751,761	12/29/2000	Ronald D. Smith	2207/10119	5065

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,761	SMITH, RONALD D.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 6/22/2004.

Withdrawn Rejections

3. Applicant, via amendment, has overcome the 35 U.S.C. 112 rejections set forth in the previous Office Action. Consequently, these rejections have been withdrawn by the examiner.

Maintained Rejections

4. Applicant has failed to overcome the 35 U.S.C. 102 and 103 rejections set forth in the previous Office Action for claims 1-19. Therefore, these rejections are respectfully maintained by the examiner and copied below for applicant's convenience.

Maintained Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 5, 7, 14, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Swoboda et al., U.S. Patent No. 6,643,803 (herein referred to as Swoboda).

7. Referring to claim 1, Swoboda has taught a method for testing a processor including an execution stage comprising:

a) generating a neutral instruction. See the abstract, and note that the jammed instruction is the generated instruction. And, the instruction is neutral because a resource can be read as a result of the instruction. A read of a resource does not modify the architectural state of the processor, and therefore, a read is a neutral instruction.

b) providing said neutral instruction to the execution stage of said processor. It is inherent that an instruction must be executed.

c) executing said neutral instruction to ascertain an architectural state value for said processor. Again, from the abstract, upon execution of neutral instructions (those which result in a reading system resources), system resources are read. These system resources include registers (column 2, lines 50-51). Since registers hold values, these instructions would ascertain (read) values for the processor.

8. Referring to claim 5, Swoboda has taught a method as described in claim 1. Swoboda has further taught that the execution of said neutral instruction causes said processor to access a value stored in a register in said processor. From the abstract it is disclosed that system resources, which include registers (column 2, lines 50-51), are read when a neutral instruction is executed.

9. Referring to claim 7, Swoboda has taught a system for testing a processor including an execution stage, comprising comparison logic coupled to the execution stage of said processor,

wherein said execution stage is to execute a neutral instruction to ascertain an architectural state value for said processor. Again, from the abstract, upon execution of neutral instructions (those which result in a reading system resources), system resources are read. These system resources include registers (column 2, lines 50-51). Since registers hold values, these instructions would ascertain (read) values for the processor. In addition, it should be realized that these instructions are used for testing purposes, as described in column 2, lines 46-65. Therefore, for a test to occur, comparison logic must inherently exist in order to determine whether the test was a failure or success. There must be an expected outcome of some sorts which would be compared with the outcome obtained from executing the neutral instruction.

10. Referring to claim 14, Swoboda has taught a set of instructions residing in a storage medium (Fig.12, and note the instruction memory on the far left - "INST MEM"), said set of instructions capable of being executed in an execution stage by a processor for implementing a method to test the processor, the method comprising:

a) generating a neutral instruction. See the abstract, and note that the jammed instruction is the generated instruction. And, the instruction is neutral because a resource can be read as a result of the instruction. A read of a resource does not modify the architectural state of the processor, and therefore, a read is a neutral instruction.

b) providing said neutral instruction to the execution stage of said processor. It is inherent that an instruction must be executed.

c) executing said neutral instruction to ascertain an architectural state value for said processor. Again, from the abstract, upon execution of neutral instructions (those which result in a reading system resources), system resources are read. These system resources include registers (column

2, lines 50-51). Since registers hold values, these instructions would ascertain (read) values for the processor.

11. Referring to claim 18, Swoboda has taught a set of instructions as described in claim 14. Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 5.

Maintained Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 2, 8, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swoboda, as applied above, in view of Sato, U.S. Patent No. 5,903,768.

14. Referring to claim 2, Swoboda has taught a method as described in claim 1. Swoboda has not taught that said neutral instruction is generated when a plurality of instructions are generated by a compiler. However, Sato has taught such a concept. More specifically, in column 2, lines 4-13, Sato discloses that a compiler is used to generate instructions and the order in which they are executed. Furthermore, when a hazard between two instructions cannot be eliminated, the compiler inserts a NOP instruction between them to overcome the hazard. This is equivalent to generating a neutral instruction because the neutral instruction is the same as a NOP in the sense that it does not affect the architectural state of the processor. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Swoboda in view of Sato such that a neutral instruction is generated when a plurality of

instructions are generated by the compiler. This would be obvious because Sato has taught the known concept of overcoming a hazard by generating NOPs (or neutral instructions), and hazards must be overcome in order to prevent data corruption.

15. Referring to claim 8, Swoboda has taught a system as described in claim 7. Furthermore, claim 8 is rejected for the same reasons set forth in claim 2.

16. Referring to claim 15, Swoboda has taught a set of instructions as described in claim 14. Furthermore, claim 15 is rejected for the same reasons set forth in claim 2.

17. Claims 3-4, 6, 9-11, 16-17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swoboda, as applied above, in view of Mandyam et al., U.S. Patent No. 6,285,974 (herein referred to as Mandyam).

18. Referring to claim 3, Swoboda has taught a method as described in claim 1. Swoboda has not taught that said neutral instruction is generated by a No-operation (NOP) pseudo-random generator. However, Mandyam has taught generating test instructions using a random test generator. A person of ordinary skill in the art would have recognized that by implementing a random generator to generate instructions, sources of bias are eliminated. Consequently, truly random instructions may be generated which would allow for the possibility of testing any register at any appropriate point within the execution. As a result, in order to perform random testing, as opposed to biased testing, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Swoboda in view of Mandyam such that a No-operation (neutral instruction) pseudo-random generator is used to generate neutral instructions.

19. Referring to claim 4, Swoboda in view of Mandyam has taught a method as described in claim 3. Swoboda has further taught that the execution of said neutral instruction causes said processor to access a value stored in a register in said processor. From the abstract it is disclosed that system resources, which include registers (column 2, lines 50-51), are read when a neutral instruction is executed.

20. Referring to claim 6, Swoboda has taught a method as described in claim 1. Swoboda has not taught that said neutral instruction is generated by a post-processor device. However, Mandyam has taught such a concept. See Fig.3 and column 6, lines 10-14. Note that a post-processor is used to generate instructions which are used to perform a self-check. This allows for detection of architectural violations as described in column 6, lines 10-25. Since Mandyam has taught that test instructions may be generated by a post-processor, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a post-processor in Swoboda for such a purpose.

21. Referring to claim 9, Swoboda has taught a system as described in claim 7. Furthermore, claim 9 is rejected for the same reasons set forth in the rejection of claim 3.

22. Referring to claim 10, Swoboda in view of Mandyam has taught a system as described in claim 9. Furthermore, claim 10 is rejected for the same reasons set forth in the rejection of claim 4.

23. Referring to claim 11, Swoboda in view of Mandyam has taught a system as described in claim 10. Swoboda in view of Mandyam has not taught that said neutral instruction includes XORing the contents of said register with itself. However, an XOR operation is well known and accepted in the art. And, an operand of an XOR operation can be an operand of all 0's, an

operand of all 1's, and everything in between. Clearly, one of these values will be equal to the value is said register. Consequently, since an XOR operation is a fundamental logic operation, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the function of XORing the contents of a register with itself

24. Referring to claim 16, Swoboda has taught a set of instructions as described in claim 14. Furthermore, claim 16 is rejected for the same reasons set forth in the rejection of claim 3.

25. Referring to claim 17, Swoboda in view of Mandyam has taught a set of instructions as described in claim 16. Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 4.

26. Referring to claim 19, Swoboda has taught a set of instructions as described in claim 14. Furthermore, claim 19 is rejected for the same reasons set forth in the rejection of claim 6.

27. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swoboda in view of Mandyam, as applied above, in view of Hennessy and Patterson, Computer Organization and Design, 2nd Edition, 1998 (herein referred to as Hennessy).

28. Referring to claim 12, Swoboda in view of Mandyam has taught a system as described in claim 10. Swoboda in view of Mandyam has not taught that said neutral instruction includes ANDing the contents of said register with all binary 1 values. However, an AND operation is well known and accepted in the art, and supported by Hennessy. See pages 225-226. Hennessy has taught that each resulting bit will be 1 only if both corresponding operand bits are 1. And, an operand of an AND operation can be an operand of all 0's, an operand of all 1's, and everything in between. Masking (ANDing operation) is used to isolate fields, which in turn allows for the

examination of bits within a word. Consequently, since an AND operation is a fundamental logic operation, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the function of ANDing the contents of a register with all binary 1 values, as taught by Hennessy.

29. Referring to claim 13, Swoboda in view of Mandyam has taught a system as described in claim 10. Swoboda in view of Mandyam has not taught that said neutral instruction includes ORing the contents of said register with all binary 0 values. However, an OR operation is well known and accepted in the art, and supported by Hennessy. See pages 225 and 227. Hennessy has taught that each resulting bit will be 1 if either one of the corresponding operand bits are 1. And, an operand of an OR operation can be an operand of all 0's, an operand of all 1's, and everything in between. Consequently, since an OR operation is a fundamental logic operation, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the function of ORing the contents of a register with all binary 0 values, as taught by Hennessy.

Response to Arguments

30. Applicant's arguments filed on June 22, 2004, have been fully considered but they are not persuasive.

31. Applicant argues the novelty/rejection of claims 1, 7, and 14 on pages 10-11 of the remarks, in substance that:

> "Swoboda does not disclose an execution stage of a processor to execute a neutral instruction to ascertain an architectural state value for the processor, as recited by claims 1, 7, and 14."
>
> "The instruction in question causes the processor to be read, but Swoboda does not state that the instruction is a read instruction, or that the processor executes the read."

> "In other words, the read is performed by the debug architecture, and not by the processor execution stage. Furthermore, Swoboda does not indicate that the state is not altered by these instructions. Therefore, Swoboda does not disclose the execution stage of a processor executing a neutral instruction to ascertain an architectural state value for the processor. Applicants respectfully submit, therefore, that elements of claim 1, 7, and 14 are neither shown nor suggested by the cited reference."

32. These arguments are not found persuasive for the following reasons:

a) To clarify, applicant's attention is directed towards claim 4 of Swoboda. Note that a null instruction (neutral instruction) is generated and jammed into the processor's instruction pipeline (also shown in Fig.16). As stated in the rejection of claim 1, the neutral instruction would inherently be executed because all instructions within a processor pipeline are executed. This in turn causes a bubble in the pipeline, which is disclosed in Swoboda's claim 4. When the bubble is detected, the test port circuitry is able to ascertain a value of a register. By waiting for a bubble, the instruction pipeline will not be accessing the desired system resource (see claim 1), so it may be read without interfering with the processor's execution. Also, it should be realized from claim 1 that Swoboda's processor comprises the test port circuitry, the emulation circuitry, the detection circuitry, and the jamming circuitry, in addition to the expected instruction pipeline and system resources. Consequently, even if applicant is correct in saying the emulation circuitry does the reading of the resource, the emulation circuitry is still part of the processor according to Swoboda. Hence, the processor does the reading. Overall, the generation, providing, and execution of the neutral (null) instruction allows for the reading of an architectural value of the processor.

Conclusion

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
July 15, 2004

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